

# MOS FIELD EFFECT TRANSISTOR

# $\mu$ PA2701GR

## SWITCHING

### N-CHANNEL POWER MOS FET

#### DESCRIPTION

The  $\mu$ PA2701GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

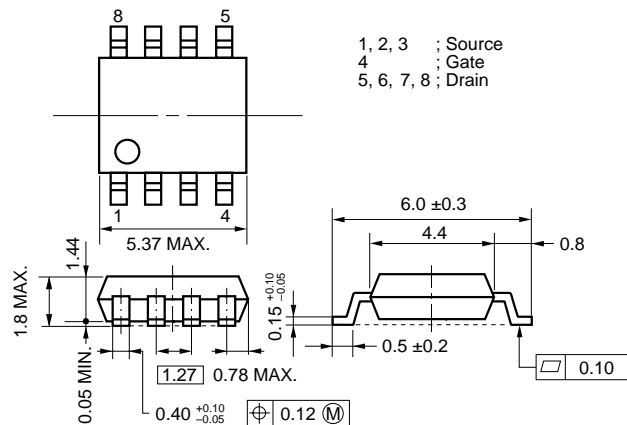
#### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 7.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$   
 $R_{DS(on)2} = 11.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1200 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA2701GR	Power SOP8

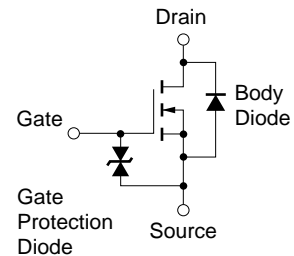
#### PACKAGE DRAWING (Unit: mm)



#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 14$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 56$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	14	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	19.6	mJ

#### EQUIVALENT CIRCUIT



- Notes**
1.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$
  2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu\text{H}$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

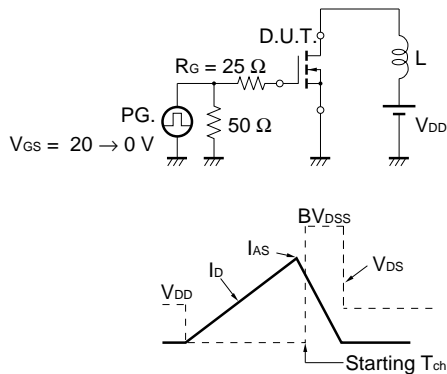
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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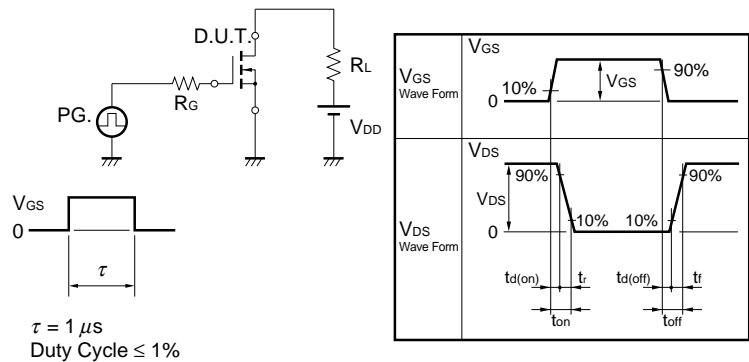
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.0 A	7	14		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.0 A		6.2	7.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.0 A		8.7	11.6	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 7.0 A		10.3	13.7	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		1200		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		500		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		160		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 7.0 A		10		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		13		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		44		ns
Fall Time	t <sub>f</sub>			11		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V		12		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		4		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 14 A		6		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 V		32		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		27		nC

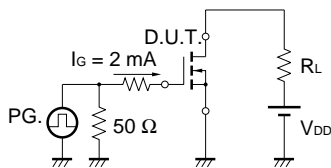
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

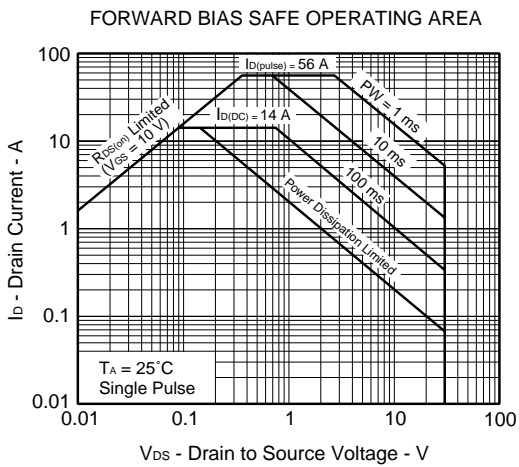
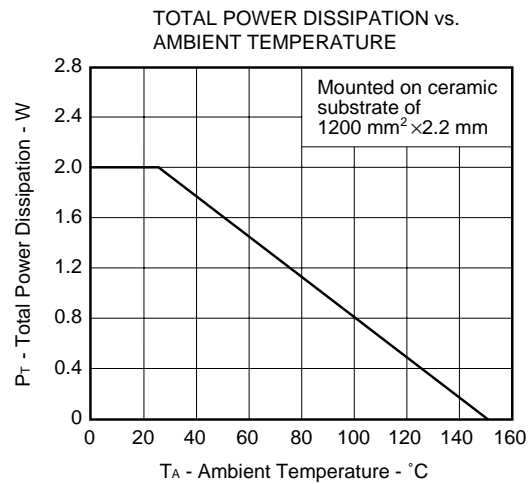
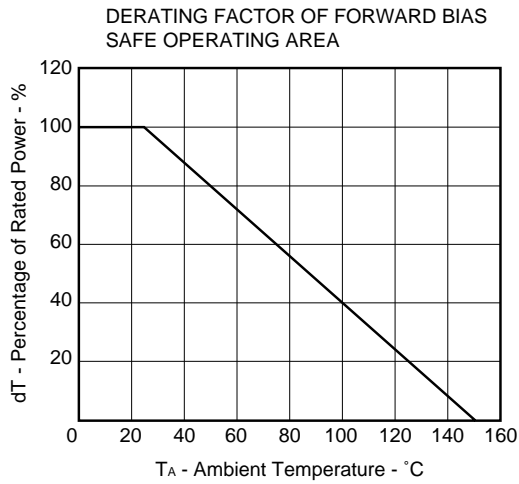


**TEST CIRCUIT 3 GATE CHARGE**

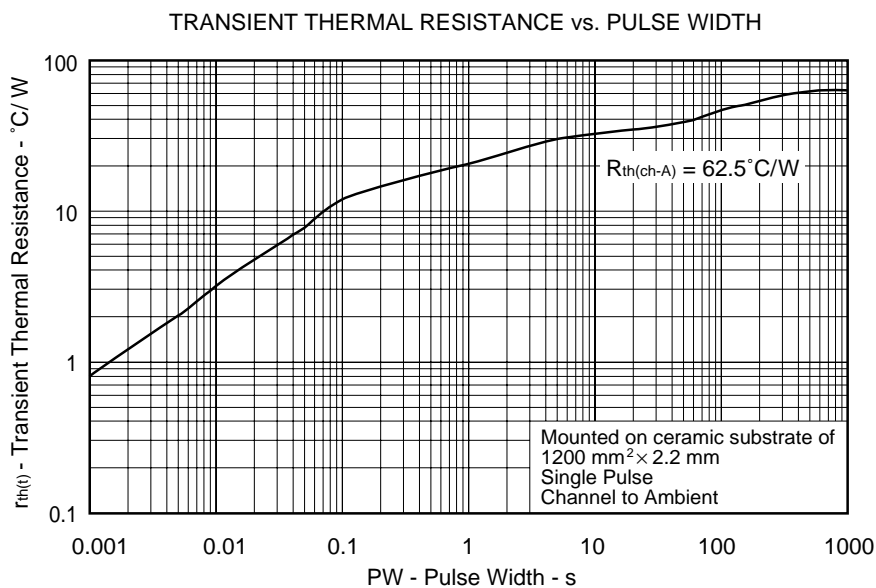


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

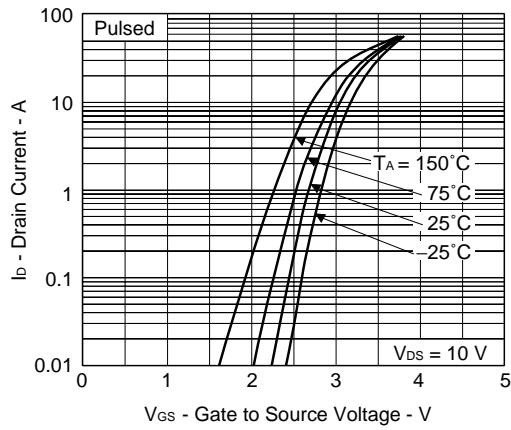
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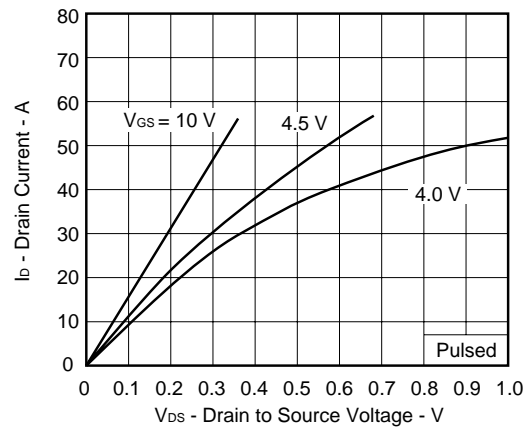
Remark Mounted on ceramic substrate of 1200 mm<sup>2</sup> × 2.2 mm



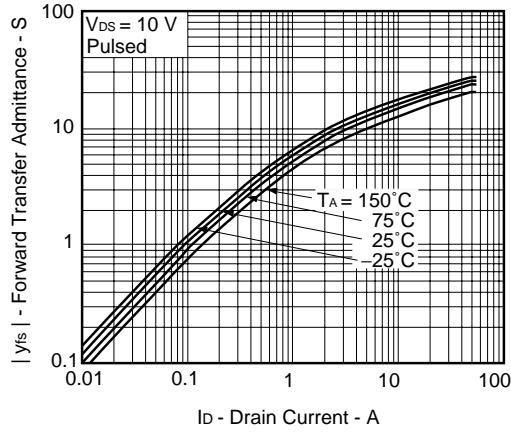
FORWARD TRANSFER CHARACTERISTICS



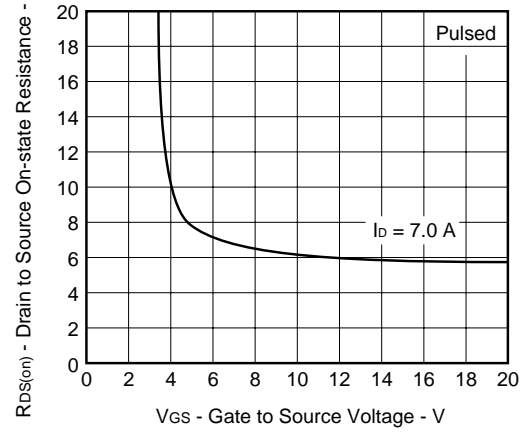
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



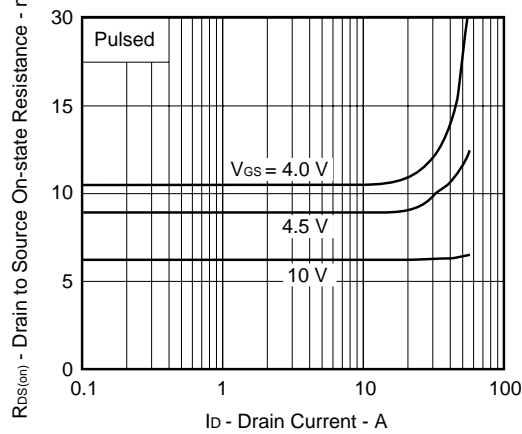
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



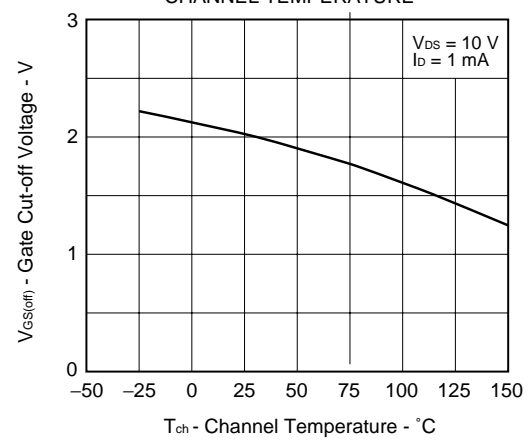
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

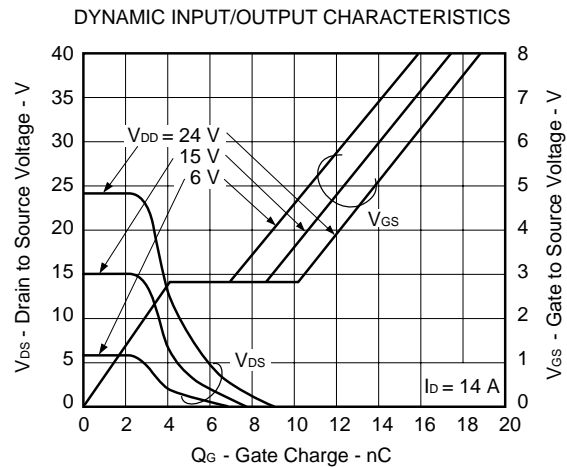
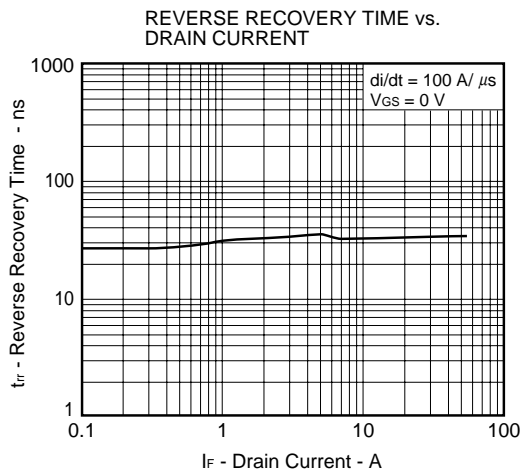
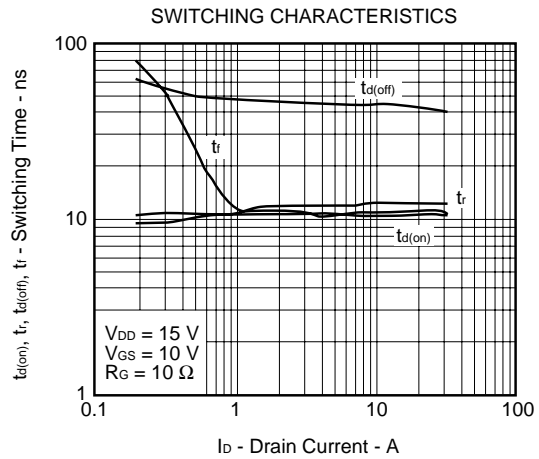
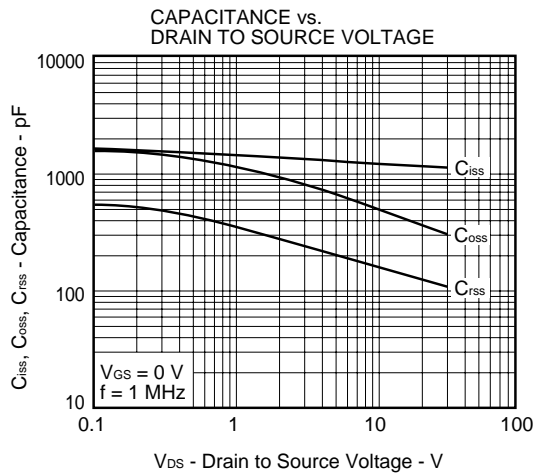
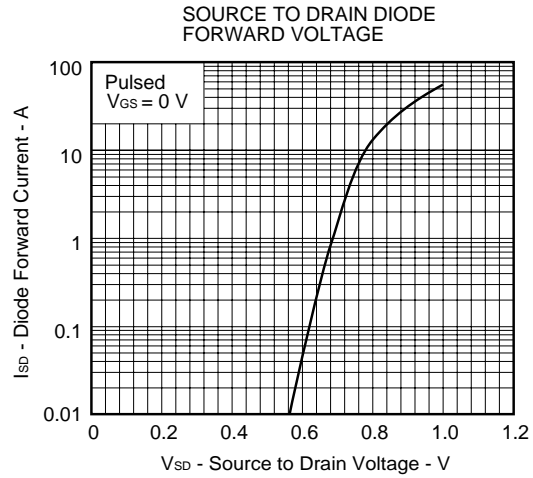
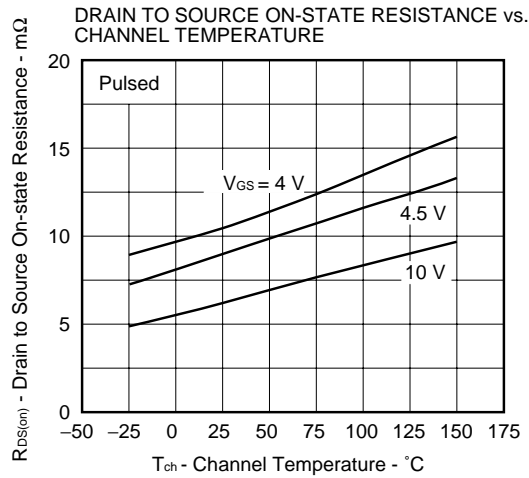


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





[MEMO]

[MEMO]

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